REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. Claims 1-27 are pending.

Oath/Declaration

The Office Action requested a new oath or declaration in compliance with 37 CFR 1.67(a). Accordingly, with this paper, Applicant encloses a Declaration and Power of Attorney for the above-identified Patent Application.

Shishizuka and Mussemann

Claims 1-7, 10-19 and 22-27 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shishizuka (U.S. 6,347,202) (Shishizuka), in view of Mussemann (U.S. 5,471,625) (Mussemann). Applicant respectfully traverses this rejection on the grounds that the combination of Shishizuka and Mussemann fails to create a *prima facie* case of obviousness.

As the PTO recognizes in MPEP §2142:

> The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

The USPTO clearly cannot establish a *prima facie* case of obviousness in connection with the amended claims for the following reasons.

35 U.S.C. §103(a) provides that:

> [a] patent may not be obtained ... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains ... (emphasis added)

Thus, when evaluating a claim for determining obviousness, all limitations of the claim must be evaluated. However, the references, alone, or in combination, do not teach the claim 1 recitation "in response to failing to detect an access request for the bus mastering device within a predetermined period of time, suspending a bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states."

The Office Action points to Figure 88 of Shishizuka as disclosing "in response to failing to detect an access request for the bus mastering device within a predetermined period of time, suspending a bus mastering device controller." Applicant respectfully disagrees and could not find a section in Shishizuka where a bus mastering device controller is suspended. The device that shifts states in Shishizuka is not a bus mastering device controller. Furthermore, in Shishizuka the bus agent waiting for the access request self-shifts transparently into and out of the low power mode. According to Shishizuka at Figure 88, "even in the sleep state, the decoder and the clock control sections [of the bus agent] are operating and wait for a request while monitoring the bus. When the decoder detects an address of itself, it opens the clock gate to operate a clock of an internal logic and responds to a bus request. The bus agent shifts to the wakeup state." However, what is currently claimed is suspending a bus mastering device controller when no access request for the bus mastering device is detected.

Mussemann teaches nothing to overcome the deficiencies pointed out above regarding Shishizuka. According to the Office Action, "Musemann teaches that operation of a bus mastering device can be suspended by a bus mastering device controller." However, what is claimed is suspending the bus mastering device controller, not suspending the bus mastering device. The Office Action also states that "[the bus mastering device controller] no longer prevents [a processor from entering a low power state] when the processor can enter the low power state." According to Mussemann, the controller can "delay the process from entering into a low-power mode of operation until a more opportune time." Mussemann col. 6, ll. 21-23. This does not disclose suspending a bus mastering device controller. Additionally, Applicant could not find any section in Shishizuka or Mussemann disclosing that the suspended controller no longer prevents the processor from entering low power states. As a result, the USPTO's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to representative claim 1. Independent claims 14, 26 and 27 are patentable at least for similar reasons as described for representative claim 1.

As to claim 6, the Office Action states that "Shishizuka discloses detecting an access request for the bus mastering device, starting the timer for the predetermined period of time, and resuming the operation of the bus mastering device controller are performed in response to an executable code executable by the IHS." The executable code is executed by a processor within the IHS. In embodiments mentioned in the current application, the filter driver (executable code) when executed by the processor can do a variety of tasks such as, for example, starting a timer for a period of time, clearing a USB state flag, setting a USB state flag,

monitoring input/output request packets generated for the controller, monitoring input/output request packets, determining whether USB controller is currently in suspend mode, and causing the USB controller to be placed into suspend mode. Paragraphs 19-22. Applicant could find no mention of executable code run by any processor in Shishizuka Figure 88. Similar arguments further support the patentability of claims 7-8 and 14-27.

Therefore, it is impossible to render the subject matter of the claims as a whole obvious based on a single reference or any combination of the references, and the above explicit terms of the statute cannot be met. As a result, the USPTO's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to the claims, and a rejection under 35 U.S.C. §103(a) is not applicable to claims 1, 14, 26 and 27, and to the claims which depend therefrom.

There is still another compelling, and mutually exclusive, reason why the references cannot be combined and applied to reject the claims under 35 U.S.C. §103(a).

The PTO also provides in MPEP §2142:

> [T]he Examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the Examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. ...[I]mpermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

Here, the references do not teach, or even suggest, the desirability of the combination because neither teaches nor suggests suspending a bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states. Claims 14, 26 and 27 are patentable for similar reasons as described for representative claim 1.

Thus, neither of these references provides any incentive or motivation supporting the desirability of the combination. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. §103(a) rejection of claims 1, 14, 26 and 27, and to the claims which depend therefrom.

In this context, the MPEP further provides at §2143.01:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (emphasis in original)

In the above context, the courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In the present case it is clear that the USPTO's combination arises solely from hindsight based on the invention without any showing, suggestion, incentive or motivation in either reference for the combination as applied to the claims. Therefore, for this mutually exclusive reason, the USPTO's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to the claims.

Shishizuka, Mussemann, and Applicant's Admitted Prior Art

Claims 8-9 and 20-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shishizuka (U.S. 6,347,202) (Shishizuka), in view of Mussemann (U.S. 5,471,625) (Mussemann), in further view of Applicant's Admitted Prior Art. This combination of references cannot establish a *prima facie* case of obviousness for the claims, which depend from claims 1 and 14, because Applicant's Admitted Prior Art teaches nothing to overcome the deficiencies noted above for Shishizuka and Mussemann. Applicant respectfully requests that the rejection be withdrawn and the claims allowed.

In view of all of the above, the allowance of claims 1-27 is respectfully requested.

The Examiner is invited to call the undersigned at the below-listed telephone number if a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

James R. Bell
Registration No. 26,528

Dated: 12-20-06

HAYNES AND BOONE, LLP
901 Main Street, Suite 3100
Dallas, Texas 75202-3789
Telephone: 512/867-8407
Facsimile: 214/200-0853
ipdocketing@haynesboone.com

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office, via EFS-Web, on the date indicated below:

on December 20, 2006
Date

Susan C. Lien
Susan C. Lien